Examination Period 2: 2018/19

<table>
<thead>
<tr>
<th>Module Title</th>
<th>Advanced Digital Electronics</th>
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<tbody>
<tr>
<td>Level</td>
<td>Six</td>
</tr>
<tr>
<td>Time Allowed</td>
<td>Two hours</td>
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Instructions to students:
- Enter your student number **not** your name on all answer books.
- Answer **all** questions.
- All questions are equally weighted. Where a question has more than one part the division of marks is stated.
- Begin each question on a separate answer page; label each answer page clearly with the number of the question you are answering.
- The use of a calculator **is** permitted.
- Graph paper can be found at the back of each answer book.
- Formulae is provided at the back of this exam paper.

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<th>No. of Pages</th>
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Answer all questions.

Question 1

a. What device is described by the VHDL code shown in Figure Q1.1? 
   (12 marks)

b. Design the logic diagram using 2-input logic gates of a 4 by 1 multiplexer. 
   (15 marks)

c. Implement an XNOR gate with a 4 by 1 multiplexer.
   (13 marks)

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity componentX is
   generic (N : integer := 8);
   port ( clr : in STD_LOGIC;
          clk : in STD_LOGIC;
          q: out STD_LOGIC_VECTOR (N-1 downto 0) );
end componentX;

architecture componentX of componentX is
   signal a: STD_LOGIC_VECTOR (N-1 downto 0);
begin
   process (clk, clr)
   begin
     if clr = '1' then
       a <= (others => '0');
     elseif clk'event and clk = '1' then
       a <= a + 1;
     end if;
   end process;
   q <= a;
end componentX;

Figure Q1.1

Total: 40 marks
Question 2

a. Explain the difference between a combinational and a sequential logic circuit. (5 marks)

b. Highlight the main difference between Moore and Mealy clocked sequential circuits. (5 marks)

c. For the state diagram in Figure Q2.1, answer the following questions:

i. how many D-flip-flops will this machine take if the states are encoded in **binary**? (2 marks)

ii. how many D-flip-flops will this machine take if the states are encoded in **gray code**? (3 marks)

iii. how many D-flip-flops will this machine take if the states are encoded in **one-hot**? (3 marks)

iv. is this a Mealy or a Moore Machine? (2 marks)

v. construct the next-state table for the state diagram in Figure Q2.1. (10 marks)

vi. design the final simplified circuit using D-type flip-flops. (15 marks)

vii. design the final simplified circuit using J-K flip-flops. (15 marks)

![Figure Q2.1](image)

Total: 60 marks

End of Questions
Formulae follows overleaf
Formulae

Basic rules of Boolean algebra.

1. $A + 0 = A$
2. $A + 1 = 1$
3. $A + 0 = 0$
4. $A + 1 = 1$
5. $A + A = A$
6. $A + A = 1$
7. $A \cdot A = A$
8. $A \cdot A = 0$
9. $\overline{A} = A$
10. $A + AB = A$
11. $A + \overline{A}B = A + B$
12. $(A + B)(A + C) = A + BC$

DeMorgan’s first theorem

The complement of a product of variables is equal to the sum of the complements of the variables.

$$\overline{XY} = \overline{X} + \overline{Y}$$

DeMorgan’s second theorem

The complement of a sum of variables is equal to the product of the complements of the variables.

$$\overline{X + Y} = \overline{X} \overline{Y}$$

Latches

![Diagram of S-R latches]

Truth table for an active-LOW input S-R latch.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\overline{S}$</td>
<td>$\overline{R}$</td>
<td>$Q$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>NC</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
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Flip-Flops

D flip-flop \( Q^+ = D \)

D-CE flip-flop \( Q^+ = D \cdot CE + Q \cdot CE' \)

T flip-flop \( Q^+ = T \oplus Q \)

S-R flip-flop \( Q^+ = S + R'Q \)

J-K flip-flop \( Q^+ = JQ' + K'Q \)

End of Formulae

End of Paper