Examination Period 3: 2017/18

ENG302218N

Module Title Advanced Digital Electronics
Level Six
Time Allowed Two hours

Instructions to students:
• Enter your student number not your name on all answer books.
• Answer all questions.
• All questions are equally weighted. Where a question has more than one part the division of marks is stated.
• Begin each question on a separate page; label each page clearly with the number of the question you are answering.
• The use of an electronic calculator is permitted.
• Graph paper will be provided or can be located at the back of each answer book.
• Relevant Formulae is included at the end of this exam paper.

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<th>No. of Pages</th>
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Answer all questions.

**Question 1**

a. What device is described by the VHDL code shown in Figure Q1.1? (12 marks)

b. Design a combinational circuit with three inputs, x, y, and z and three outputs, A, B and C.

When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input.

When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. (20 marks)

c. Use a PLA. Give the PLA table and specify the connection pattern. (8 marks)

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity componentX is
  Port (a : in STD_LOGIC_VECTOR (2 downto 0);
        y : out STD_LOGIC_VECTOR (7 downto 0));
end componentX;

architecture componentX of componentX is
begin
  process(a)
  variable j: integer;
  begin
    j := conv_integer(a);
    for i in 0 to 7 loop
      if(i = j) then
        y(i) <= '1';
      else
        y(i) <= '0';
      end if;
    end loop;
  end process;
end componentX;

Figure Q1.1
```

Total: 40 marks
Question 2

a. Explain the difference between a combinational and a sequential logic circuit. (5 marks)

b. Highlight the main difference between Moore and Mealy clocked sequential circuits. (10 marks)

c. A new flip-flop, called the UT flip-flop, has four operations:
   Reset to 0, no change, complement, and set to 1, when inputs UT are 00, 01, 10, and 11, respectively.
   i. Tabulate the characteristic table for the UT flip-flop. (5 marks)
   ii. Tabulate the excitation table for the UT flip-flop. (5 marks)
   iii. Construct the next-state table for the state diagram Figure Q2.1.
        For this problem use a D flip-flop for the MSB state bit and a UT flip-flop for the LSB state bit, and the following state assignments: S0 = 00, S1 = 01, S2 = 10, and S3 = 11. (20 marks)
   iv. Design the final simplified circuit. (15 marks)

Figure Q2.1

Total: 60 marks

End of Questions

Engineering Formulae follows overleaf
ENG3022 Formulae (EE BEng)

Basic rules of Boolean algebra.

1. \( A + 0 = A \)
2. \( A + 1 = 1 \)
3. \( A \cdot 0 = 0 \)
4. \( A \cdot 1 = A \)
5. \( A + A = A \)
6. \( A + \bar{A} = 1 \)
7. \( A \cdot A = A \)
8. \( A \cdot \bar{A} = 0 \)
9. \( \bar{A} = A \)
10. \( A + AB = A \)
11. \( A + \bar{A}B = A + B \)
12. \((A + B)(A + C) = A + BC\)

DeMorgan’s first theorem

The complement of a product of variables is equal to the sum of the complements of the variables.

\[ \overline{XY} = \overline{X} + \overline{Y} \]

DeMorgan’s second theorem

The complement of a sum of variables is equal to the product of the complements of the variables.

\[ \overline{X + Y} = \overline{XY} \]

LATCHES

![Truth table for an active-LOW input S-R latch.](image)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S )</td>
<td>( \bar{R} )</td>
<td>( Q )</td>
</tr>
<tr>
<td>1 0 1 0 0 0</td>
<td>1 1 1 1</td>
<td>NC</td>
</tr>
<tr>
<td>1 0 1 0 0 0</td>
<td>1 1 1 1</td>
<td>0</td>
</tr>
<tr>
<td>0 1 0 1 1 1</td>
<td>1 1 1 1</td>
<td>0 1</td>
</tr>
<tr>
<td>0 1 0 1 1 1</td>
<td>1 1 1 1</td>
<td>1</td>
</tr>
</tbody>
</table>
FLIP-FLOPS

Truth table for a positive edge-triggered J-K flip-flop.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>J</td>
<td>K</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ Q_{0} = \text{output level prior to clock transition} \]

\[ \uparrow = \text{clock transition LOW to HIGH} \]

Truth table for a positive edge-triggered D flip-flop.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>CLK</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ \uparrow = \text{clock transition LOW to HIGH} \]

D flip-flop \( Q^{+} = D \)

D-CE flip-flop \( Q^{+} = D\cdot CE + Q\cdot CE' \)

T flip-flop \( Q^{+} = T\oplus Q \)

S-R flip-flop \( Q^{+} = S + R'Q \)

J-K flip-flop \( Q^{+} = JQ' + K'Q \)