Examination Period 3: 2017/18

ENG205118NB

Module Title Analogue and Digital Electronics
Level Five
Time Allowed Two hours

Instructions to students:

- Enter your student number not your name on all answer books.
- Answer four questions: two from Section A and two from Section B.
- Begin each question in a separate answer book; label each answer book clearly with the number of the question you are answering.
- All questions are equally weighted. Where a question has more than one part the division of marks is stated.
- The use of a non-programmable calculator is permitted.
- Engineering formula sheets are included at the back of the exam paper.

<table>
<thead>
<tr>
<th>No. of Pages</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Questions</td>
<td>6</td>
</tr>
</tbody>
</table>

Page 1 of 16
Answer two out of three questions.

**Question 1**

**a.** The circuit in Figure Q1.1 is a diode clipper. Find the voltage across the load $R_1$. Use the practical diode approximation with the diode barrier potential of 0.7V.

(10 marks)

**b.** The circuit in Figure Q1.2 is a loaded Zener regulator. Determine the minimum and maximum permissible load currents. $V_1$ is 18V, $R_1$ is 120Ω and the zener diode is 1N4743A. Information about this Zener diode is shown in Figure Q1.3.

(15 marks)
### Absolute Maximum Ratings *

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
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<tbody>
<tr>
<td>$P_D$</td>
<td>Power Dissipation</td>
<td>1.0</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>@ $T_J \leq 50^\circ C$, Lead Length = 3/8&quot;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Derate above $50^\circ C$</td>
<td>0.07</td>
<td>mW/°C</td>
</tr>
<tr>
<td>$T_J, T_{ST}$</td>
<td>Operating and Storage Temperature Range</td>
<td>-55 to +200</td>
<td>°C</td>
</tr>
</tbody>
</table>

* These ratings are limiting values above which the serviceability of the diode may be impaired.

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#### Figure Q1.3. Zener diode datasheet

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_Z$ (V) @ $I_Z$ (Note 1)</th>
<th>Test Current $I_Z$ (mA)</th>
<th>Max. Zener Impedance $Z_Z$ @ $I_Z$ (Ω)</th>
<th>$I_ZK$ (mA)</th>
<th>$I_{R}$ (μA)</th>
<th>$V_R$ (V)</th>
<th>Non-Repetitive Peak Reverse Current $I_{ZSM}$ (mA) (Note 2)</th>
</tr>
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<tbody>
<tr>
<td>1N4743A</td>
<td>12.35</td>
<td>13</td>
<td>13.65</td>
<td>19</td>
<td>10</td>
<td>0.25</td>
<td>5 9.9 344</td>
</tr>
<tr>
<td>1N4744A</td>
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<td>15</td>
<td>15.75</td>
<td>17</td>
<td>14</td>
<td>0.25</td>
<td>5 11.4 304</td>
</tr>
<tr>
<td>1N4745A</td>
<td>15.2</td>
<td>16</td>
<td>16.0</td>
<td>15.6</td>
<td>16</td>
<td>0.25</td>
<td>5 12.2 260</td>
</tr>
<tr>
<td>1N4746A</td>
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<td>18</td>
<td>18.9</td>
<td>14</td>
<td>20</td>
<td>0.25</td>
<td>5 13.7 250</td>
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<tr>
<td>1N4747A</td>
<td>19</td>
<td>20</td>
<td>21</td>
<td>12.5</td>
<td>22</td>
<td>0.25</td>
<td>5 15.2 225</td>
</tr>
<tr>
<td>1N4748A</td>
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<td>22</td>
<td>23.1</td>
<td>23</td>
<td>23</td>
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<td>5 16.7 205</td>
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<td>1N4749A</td>
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<td>24</td>
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<td>9.5</td>
<td>40</td>
<td>0.25</td>
<td>5 22.8 150</td>
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<tr>
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<td>33</td>
<td>34.65</td>
<td>7.5</td>
<td>45</td>
<td>0.25</td>
<td>5 25.1 135</td>
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<td>5 27.4 125</td>
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<tr>
<td>1N4754A</td>
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<td>39</td>
<td>40.95</td>
<td>6.5</td>
<td>60</td>
<td>0.25</td>
<td>5 29.7 115</td>
</tr>
<tr>
<td>1N4755A</td>
<td>40.85</td>
<td>43</td>
<td>45.15</td>
<td>6</td>
<td>70</td>
<td>0.25</td>
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</tr>
<tr>
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<td>47</td>
<td>49.35</td>
<td>5.5</td>
<td>80</td>
<td>0.25</td>
<td>5 35.8 95</td>
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<tr>
<td>1N4757A</td>
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<td>51</td>
<td>53.55</td>
<td>5</td>
<td>96</td>
<td>0.25</td>
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<td>1N4758A</td>
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<td>56</td>
<td>58.8</td>
<td>4.5</td>
<td>110</td>
<td>0.25</td>
<td>5 42.6 80</td>
</tr>
</tbody>
</table>

**Notes:**
1. Zener Voltage ($V_Z$)
2. The Zener voltage is measured with the device junction in the thermal equilibrium at the lead temperature ($T_J$) at $30^\circ C$ ± 1°C and 3/8” lead length.
3. Square-wave Reverse Surge at 8.3 max. soak time.

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**Total: 25 marks**
Question 2

A heating element driver circuit based on an NPN transistor is shown in Figure Q2.1. The NPN transistor current gain ($\beta_{DC}$) is between 40 and 100. The heating element is connected to a voltage source of 24V and the wounded wire resistance of the heating element is 100Ω. Assume that the voltage drop across the collector and the emitter when the transistor is in saturation is $V_{CE(sat)}= 0.2V$ and the voltage drop across a forward biased PN junction is 0.6V.

a. Find the minimum base current to saturate the transistor. (5 marks)

b. Determine the value of $R_B$ required to ensure saturation when $V_{IN}$ is 3V. (12 marks)

c. Draw the load line and find the maximum of power dissipated in the transistor when the DC current flowing through the heating is 0.1A. (8 marks)

Total: 25 marks
Question 3

The circuit in Figure Q3.1 is a signal conditioning circuit for temperature measurements using a resistance temperature detector (RTD). The type of RTD is a pt100. The resistance varies with temperature according to the following relationship:

\[ R_T = 100 \cdot (1 + 0.00385 \cdot t) \]

where \( t \) is in degrees centigrade \(^\circ\)C. \( V_{SS} \) is -10V.

Find the following:

a. Analyse the circuit in Figure Q3.1 and find the ratio between the output voltage and the current flowing through the pt100. (10 marks)

b. The current following through the pt100 at 0\(^\circ\)C, \( I_{Pt100}(0^\circ C) \) and 150\(^\circ\)C, \( I_{Pt100}(150^\circ C) \). (8 marks)

c. The value of \( R_f \) for an output voltage of 5V at 150\(^\circ\)C. (7 marks)

Figure Q3.1

Total: 25 marks
Section B

Answer two out of three questions.

Question 4

a. Convert the following 16-bit signed hexadecimal numbers to their decimal and binary equivalents.
   • 03B8
   • 8022  

b. Determine the truth table of the digital circuit shown in Figure Q4.1. 

![Figure Q4.1](image)

Figure Q4.1

Total: 25 marks

Question 5

Obtain the minimised SOP and POS expression for the following Boolean logic equation using Karnaugh maps:

\[ Y(A, B, C, D) = (A + B + D)(\overline{A} + C + D) \]

(25 marks)
Question 6

A half subtractor is used for subtracting one single bit binary digit from another single bit binary digit. The half subtractor has two inputs A and B and two output signals Difference (D) and Borrow (B). The output signal D is A minus B and the output signal borrow indicates if after performing a subtraction the result is negative or positive.

For example if A is 0 and B is 1, D is 1 and borrow is 1.

**Implement a half subtractor circuit:**

a. Determine the truth table.  
   (8 marks)

b. Simplify if possible, the SOP expression using Karnaugh Maps.  
   (10 marks)

c. Draw the simplified logic diagram using logic gates of two inputs.  
   (7 marks)

Total: 25 marks
**Complex Numbers:**

\[ Z = a + jb; \quad Z = r \angle \theta \]

\[ r = \sqrt{a^2 + b^2}; \quad \theta = \tan^{-1} \frac{b}{a} \]

**Resonance:**

\[ f_0 = \frac{1}{2\pi \sqrt{LC}} \]

**Capacitor with an Initial voltage. Voltage growth in RC circuits:**

\[ \tau = RC \]

\[ v_c = E + (V_0 - E)e^{\frac{t}{\tau}} \]

\[ i_c = \frac{(E - V_0)}{R} e^{\frac{t}{\tau}} \]

**Capacitor discharging equations:**

\[ \tau = RC \]

\[ v_c = V_0 e^{-\frac{t}{\tau}} \]

\[ i_c = -\frac{V_0}{R} e^{-\frac{t}{\tau}} \]

**Current Buildup Transients. RL circuit:**

\[ \tau = \frac{L}{R} \]

\[ v_L = E e^{-\frac{t}{\tau}} \]

\[ i = \frac{E}{R} \left(1 - e^{-\frac{t}{\tau}}\right) \]

**De-energizing transients. RL decay transients:**

\[ i = I_0 \cdot e^{\frac{t}{\tau}} \]

**Universal voltage and current curves for RC circuits:**

**Universal voltage and current curves for RL circuits:**
Relationship between $\omega$, $T$, and $f$:

$$\omega T = 2\pi \left( \text{rad} \right)$$

$$\omega = \frac{2\pi}{T} \left( \frac{\text{rad}}{\text{s}} \right) = 2\pi f \left( \frac{\text{rad}}{\text{s}} \right)$$

Impedance:

$$Z = \frac{V}{I} \begin{cases} 
R \text{ for a resistor} \\
j \omega L \text{ for an ideal inductor} \\
\frac{1}{j \omega C} \text{ for an ideal capacitor}
\end{cases}$$

The Power Triangle:

$$S = P + jQ$$

$$P = V \cdot I \cdot \cos(\theta) = S \cdot \cos(\theta)$$

$$Q = V \cdot I \cdot \sin(\theta) = S \cdot \sin(\theta)$$

Power factor:

$$F_p = \cos(\theta)$$

Amplifiers:

$$A_v = 20 \log_{10} \frac{V_{out}}{V_{in}} \text{ dB}$$

$$A_v(f) = \frac{A_v}{1 + \beta A_v}$$

$$A_p = 10 \log_{10} \frac{P_{out}}{P_{in}} \text{ dB}$$

$$CMRR = \frac{A_v(\text{diff})}{A_v(\text{com})}$$

Power supplies:

$$\Delta V = \frac{I_{\text{load}}}{2fC}$$

Transformer:

$$\frac{I_1}{I_2} \approx \frac{N_2}{N_1} \approx \frac{V_2}{V_1}$$

Formula sheets continue overleaf
## Analogue Fundamentals

### Half Way Rectifier

- **Peak value of output:**
  \[ V_{p(out)} = V_{p(sec)} - 0.7 \text{ V} \]
- **Average value of output:**
  \[ V_{AVG} = \frac{V_{p(out)}}{\pi} \]
- **Diode peak inverse voltage:**
  \[ PIV = V_{p(sec)} \]

### Centre-Tapped Full Way Rectifier

- **Peak value of output:**
  \[ V_{p(out)} = \frac{V_{p(sec)}}{2} - 0.7 \text{ V} \]
- **Average value of output:**
  \[ V_{AVG} = \frac{2V_{p(out)}}{\pi} \]
- **Diode peak inverse voltage:**
  \[ PIV = 2V_{p(out)} + 0.7 \text{ V} \]

### Bridge Full Way Rectifier

- **Peak value of output:**
  \[ V_{p(out)} = V_{p(sec)} - 1.4 \text{ V} \]
- **Average value of output:**
  \[ V_{AVG} = \frac{2V_{p(out)}}{\pi} \]
- **Diode peak inverse voltage:**
  \[ PIV = V_{p(out)} + 0.7 \text{ V} \]
Transistor Bias Circuits (NPN)

\[ V_B = V_B + V_{BE} \]
\[ V_C = V_{CC} - I_C R_C \]
\[ V_E = I_E R_E \]
\[ I_C = I_E \]
\[ I_B = \frac{V_B}{R_{IN(BASE)}} \]

\[ V_B = V_E + V_{BE} \]
\[ I_E = \frac{V_{TH} - V_{BE}}{R_E + \frac{R_{TH}}{R_{DC}}} \]
\[ I_C = I_E \]
\[ I_B = \frac{V_B}{R_{IN(BASE)}} \]

\[ V_C = V_{CC} - I_C R_C \]
\[ V_E = V_{EE} + I_E R_E \]
\[ I_C = I_E \]
\[ I_B = \frac{V_B}{R_B} \]

\[ V_C = V_{CC} - I_C R_C \]
\[ V_E = 0 \text{ V} \]
\[ I_C = \beta_{DC} \left( \frac{V_{CC} - V_{BE}}{R_B} \right) \]
\[ I_E = I_C \]
\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]

\[ V_B = I_B R_E + V_{BE} \]
\[ V_C = V_{CC} - I_C R_C \]
\[ V_E = V_B - V_{BE} \]
\[ I_E = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_{TH}}{R_{DC}}} \]
\[ I_C = I_E \]
\[ I_B = \frac{V_{CC} - V_B}{R_B} \]

Formula sheets continue overleaf
Common-Emitter Amplifier

\[ r'_e \equiv \frac{25 \text{ mV}}{I_E} \quad \text{Internal ac emitter resistance} \]

\[ R_{\text{in(base)}} = R_1 \parallel R_2 \parallel R_{\text{in(base)}} \quad \text{Total amplifier input resistance, voltage-divider bias} \]

\[ R_{\text{in(base)}} = \beta_{ac} r'_e \quad \text{Input resistance at base} \]

\[ R_{\text{out}} \equiv R_C \quad \text{Output resistance} \]

\[ A_v = \frac{R_C}{r'_e} \quad \text{Voltage gain, base-to-collector, unloaded} \]

\[ A_v = \frac{R_C}{r'_e + R_E} \quad \text{Voltage gain without bypass capacitor} \]

\[ A_v = \frac{R_C}{r'_e} \quad \text{Voltage gain, base-to-collector, loaded, bypassed } R_E \]

\[ A_v \equiv \frac{R_C}{R_{E1}} \quad \text{Voltage gain, swamped amplifier} \]

\[ R_{\text{in(base)}} = \beta_{ac}(r'_e + R_{E1}) \quad \text{Input resistance at base, swamped amplifier} \]

\[ A_i = \frac{I_c}{I_s} \quad \text{Current gain, input source to collector} \]

\[ A_p = A_v A_i \quad \text{Power gain} \]

Common-Collector Amplifier

\[ A_v \equiv 1 \quad \text{Voltage gain, base-to-emitter} \]

\[ R_{\text{in(base)}} \equiv \beta_{ac} R_e \quad \text{Input resistance at base, loaded} \]

\[ R_{\text{out}} \equiv \left( \frac{R_s}{\beta_{ac}} \right) \parallel R_E \quad \text{Output resistance} \]

\[ A_i = \frac{I_c}{I_{\text{in}}} \quad \text{Current gain} \]

\[ A_p \equiv A_i \quad \text{Power gain} \]

\[ R_{\text{in}} = \beta_{ac1} \beta_{ac2} R_E \quad \text{Input resistance, Darlington pair} \]

Common-Base Amplifier

\[ A_v \equiv \frac{R_C}{r'_e} \quad \text{Voltage gain, emitter-to-collector} \]

\[ R_{\text{in(emitter)}} \equiv r'_e \quad \text{Input resistance at emitter} \]

\[ R_{\text{out}} \equiv R_C \quad \text{Output resistance} \]

\[ A_i \equiv 1 \quad \text{Current gain} \]

\[ A_p \equiv A_v \quad \text{Power gain} \]

Formula sheets continue overleaf
Multistage Amplifier

\[ A_v = A_{v1} A_{v2} A_{v3} \ldots A_{vn} \quad \text{Overall voltage gain} \]

\[ A_{v\text{dB}} = 20 \log A_v \quad \text{Voltage gain expressed in dB} \]

Op-Amp Input Modes and Parameters

\[ \text{CMRR} = \frac{A_{ol}}{A_{cm}} \quad \text{Common-mode rejection ratio} \]

\[ \text{CMRR} = 20 \log \left( \frac{A_{ol}}{A_{cm}} \right) \quad \text{Common-mode rejection ratio (dB)} \]

\[ I_{\text{BIAS}} = \frac{I_1 + I_2}{2} \quad \text{Input bias current} \]

\[ I_{\text{OS}} = |I_1 - I_2| \quad \text{Input offset current} \]

\[ V_{OS} = I_{OS} R_{in} \quad \text{Offset voltage} \]

\[ V_{OUT(error)} = A_v I_{OS} R_{in} \quad \text{Output error voltage} \]

\[ \text{Slew rate} = \frac{\Delta V_{out}}{\Delta t} \quad \text{Slew rate} \]

Op-Amp Configurations

\[ A_{cl(NI)} = 1 + \frac{R_f}{R_i} \quad \text{Voltage gain (noninverting)} \]

\[ A_{cl(VF)} = 1 \quad \text{Voltage gain (voltage-follower)} \]

\[ A_{cl(I)} = -\frac{R_f}{R_i} \quad \text{Voltage gain (inverting)} \]

Op-Amp Impedances

\[ Z_{in(NI)} = (1 + A_{ol}B) Z_{in} \quad \text{Input impedance (noninverting)} \]

\[ Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol}B} \quad \text{Output impedance (noninverting)} \]

\[ Z_{in(VF)} = (1 + A_{ol}) Z_{in} \quad \text{Input impedance (voltage-follower)} \]

\[ Z_{out(VF)} = \frac{Z_{out}}{1 + A_{ol}} \quad \text{Output impedance (voltage-follower)} \]

\[ Z_{in(I)} \approx R_i \quad \text{Input impedance (inverting)} \]

\[ Z_{out(I)} = \frac{Z_{out}}{1 + A_{ol}B} \quad \text{Output impedance (inverting)} \]

Formula sheets continue overleaf
Op-Amp Frequency Responses

\[
BW = f_{cu}
\]
Op-amp bandwidth

\[
\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + f^2/f_c^2}}
\]
RC attenuation

\[
A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + f^2/f_c^2}}
\]
Open-loop voltage gain

\[
\theta = -\tan^{-1}\left(\frac{f}{f_c}\right)
\]
RC phase shift

\[
f_{c(el)} = f_{c(mid)}(1 + BA_{ol(mid)})
\]
Closed-loop critical frequency

\[
BW_{cl} = BW_{ol}(1 + BA_{ol(mid)})
\]
Closed-loop bandwidth

\[
f_T = A_{ol}f_{c(el)}
\]
Unity-gain bandwidth

Digital Electronics

Basic rules of Boolean algebra.

1. \( A + 0 = A \)
2. \( A + 1 = 1 \)
3. \( A \cdot 0 = 0 \)
4. \( A \cdot 1 = A \)
5. \( A + A = A \)
6. \( A + \overline{A} = 1 \)
7. \( A \cdot A = A \)
8. \( A \cdot \overline{A} = 0 \)
9. \( \overline{A} = A \)
10. \( A + AB = A \)
11. \( A + \overline{A}B = A + B \)
12. \( (A + B)(A + C) = A + BC \)

DeMorgan’s first theorem

The complement of a product of variables is equal to the sum of the complements of the variables

\[
\overline{XY} = \overline{X} + \overline{Y}
\]

DeMorgan’s second theorem

The complement of a sum of variables is equal to the product of the complements of the variables.

\[
\overline{X + Y} = \overline{XY}
\]
Single-Precision Floating-Point Binary Numbers

![Diagram](image)

The eight bits in the exponent represent a *biased exponent*, which is obtained by adding 127 to the actual exponent.

\[
\text{Number} = (-1)^S (1 + F)(2^{E-127})
\]

Latches

![Diagram](image)

Truth table for an active-LOW input S-R latch.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\overline{S})</td>
<td>(\overline{R})</td>
<td>(Q)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>NC</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
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<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Formula sheets continue overleaf
Flip-Flops

Truth table for a positive edge-triggered J-K flip-flop.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
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<td>J</td>
<td>K</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Q₀</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Q₀̅</td>
</tr>
</tbody>
</table>

↑ = clock transition LOW to HIGH
Q₀ = output level prior to clock transition

Truth table for a positive edge-triggered D flip-flop.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>CLK</td>
<td>Q</td>
</tr>
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<td>0</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
</tr>
</tbody>
</table>

↑ = clock transition LOW to HIGH

Next state equations of common flip-flops

D flip-flop  \[ Q^+ = D \]
S-R flip-flop \[ Q^+ = S + R'Q \]
J-K flip-flop \[ Q^+ = JQ' + K'Q \]

Internal functional diagram of a 555 timer (pin numbers are in parentheses)

End of Formula sheets
End of Paper