Examination Period 3: 2016/17

Module Title: Analogue and Digital Electronics (BSc and HND Cohort)
Level: Five
Time Allowed: Two hours

Instructions to students:
- Enter your student number **not** your name on all answer books.
- Answer **four** questions: **two** from **Section A** and **two** from **Section B**.
- All questions are equally weighted. Where a question has more than one part the division of marks is stated.
- The use of electronic calculators of an approved type is permitted.
- Mathematical formulae and graph paper will be provided.
- Students are permitted to remove this examination paper at the end of the examination.

<table>
<thead>
<tr>
<th>No. of Pages</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Questions</td>
<td>6</td>
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</table>
Section A

Answer two questions from this Section.

Question 1

The circuit shown in Figure Q1.1 is a full wave rectifier power supply with a transformer turns ratio is 10:1, and the line voltage has a frequency of 50Hz.

a. Determine the peak-to-peak ripple and dc output voltages. Assume ideal diodes in your calculations. \( R_{\text{surge}} \) is 10Ω, \( R_L \) is 5kΩ, \( C_1 \) is 100µF. (10 marks)

b. What is the purpose of \( R_{\text{surge}} \)? (5 marks)

c. A Zener-regulated DC Power supply will be used to keep a regulated DC output voltage across a variable load resistance \( R_L \). A diagram of this DC PSU is shown in Figure Q1.2. Find the range of values of \( R_L \) to keep the output voltage regulated. \( R_1 \) is 220Ω and the zener diode is 1N4746A. Information about this Zener diode is shown in Figure Q1.3. (10 marks)

Total: 25 marks

Figure Q1.1

Figure Q1.2

Page 2 of 7
### Figure Q1.2

The tolerance is 5%.

- **DO-41 Glass case**
- **Color band denotes cathode**

<table>
<thead>
<tr>
<th>Absolute Maximum Ratings *</th>
<th>T&lt;sub&gt;j&lt;/sub&gt; = 25°C unless otherwise noted</th>
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<tbody>
<tr>
<td>Symbol</td>
<td>Parameter</td>
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<tr>
<td><strong>P&lt;sub&gt;D&lt;/sub&gt;</strong></td>
<td>Power Dissipation</td>
</tr>
<tr>
<td>@ TL ≤ 50°C, Load Length = 3/8&quot;</td>
<td>1.0</td>
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<tr>
<td></td>
<td>Derate above 50°C</td>
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<tr>
<td><strong>T&lt;sub&gt;J&lt;/sub&gt;, T&lt;sub&gt;stg&lt;/sub&gt;</strong></td>
<td>Operating and Storage Temperature Range</td>
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* These ratings are limiting values above which the reliability of the diode may be impaired.

<table>
<thead>
<tr>
<th>Device</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>$V_Z$ (V) @ $I_Z$ (mA)</th>
<th>I&lt;sub&gt;z&lt;/sub&gt; (mA)</th>
<th>Max. Zener Impedance</th>
<th>Leakage Current</th>
<th>Non-Repetitive Peak Reverse Current</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(Note 1)</td>
<td></td>
<td>$Z_Z$ @ $I_Z$ (Ω)</td>
<td>$I_Z$ (mA)</td>
<td>$V_Z$ (V)</td>
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<td>1N4733A</td>
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<td>13</td>
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<td>19</td>
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<td>700</td>
<td>0.25</td>
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<td>14.25</td>
<td>15</td>
<td>15.75</td>
<td>17</td>
<td>14</td>
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<tr>
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<td>16</td>
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<td>700</td>
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<td>19</td>
<td>18.9</td>
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<td>20</td>
<td>750</td>
<td>0.25</td>
<td>5</td>
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<tr>
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<td>20</td>
<td>21</td>
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<td>750</td>
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<tr>
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<td>31.5</td>
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<td>33</td>
<td>34.65</td>
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<tr>
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<td>50</td>
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<tr>
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<td>6</td>
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<td>1500</td>
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<td>110</td>
<td>2000</td>
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Notes:
1. Zener Voltage ($V_Z$)
2. The Zener voltage is measured with the device junction in the thermal equilibrium at the load temperature ($T_J$) at 30°C ± 1°C and 3/8" lead length.
3. Square wave Reverse Surge at 0.3 max. peak time.

**Figure Q1.3.** Zener diode datasheet
Question 2

The relay driver circuit in Figure Q2.1 has an NPN transistor of current gain ($\beta_{DC}$) between 100 and 500. The relay is connected to a voltage source of 12V and the DC coil resistance is 680$\Omega$. The relay energising current is 15mA. Assume $V_{CE(sat)} = 0.2V$ and the voltage drop across a forward biased PN junction is 0.6V.

a. Determine the value of $R_B$ required to ensure saturation when $V_{IN}$ is 4V. (12 marks)

b. What must $V_{IN}$ be to cut off the transistor? (5 marks)

c. Draw the load line and find the maximum of power dissipated in the transistor when the DC current flowing through the DC coil is 10mA. (8 marks)

Total: 25 marks

Figure Q2.1
Question 3

Refer to Figure Q3.1. Determine the following:

a.  $V_{R1}$ and $V_{R2}$  
    (5 marks)

b.  Current through $R_f$  
    (5 marks)

c.  $V_{OUT}$  
    (5 marks)

d.  Find the value of $R_f$ necessary to produce an output that is five times the sum of the inputs  
    (10 marks)

Total: 25 marks

Figure Q3.1
Section B

Answer two questions from this Section.

Question 4

a. Convert the following binary numbers to their hexadecimal equivalents:
   - 1010110110111
   - 101011011001.1010100

   (10 marks)

b. Determine the faulty gates in Figure Q4.1 by analysing their timing diagrams.

   (15 marks)

Figure Q4.1
Question 5

Obtain the minimised SOP and POS expression for the following Boolean logic equation using Karnaugh maps:

\[ Y(A, B, C, D) = (A + B + C)(\overline{A} + B + D) \]

(25 marks)

Total: 25 marks

Question 6

An odd parity generator is a combinational logic circuit that generates the parity bit such that the number of 1s in the message becomes odd. The parity generator checks the input’s binary information and generates the parity bit 0/1 such that after the addition of parity bit, the total number of 1s in the message become odd.

Implement a 4-bit odd parity generator circuit:

a. Determine the truth table (8 marks)

b. Simplify if possible, the SOP expression using Karnaugh Maps (10 marks)

c. Draw the simplified logic diagram using logic gates of two inputs (7 marks)

Total: 25 marks

End of Section B
End of Paper